REMARKS

The Final Office Action mailed on May 13, 2003, has been received and reviewed.

Claims 1-67 are currently pending in the above-referenced application.

Claims 14-16, 27-30, 34-36, 41, and 45-67 have been withdrawn from consideration as being drawn to non-elected inventions.

Claims 1-13, 17-26, 31-33, 37-40, and 42-44, which have been considered, stand rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

Claims 1-11, 17-26, 31-33, 40, and 42-44 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,552,416 to Foster (hereinafter "Foster").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Foster describes a lead frame 10 which includes external lead fingers 12 and inner lead traces (ILTs) 20. Col. 3, lines 18-26. The ILTs 20 are part of the paddle 14 of the lead frame 10 (*Id.*) and are held in position relative to one another by way of "a tape [32], such as a standard lead locking tape, . . . placed over an interior portion on either side of paddle area 14" (col. 3, lines 30-33). The ILTs 20, which are obviously formed as part of the lead frame 10 and, thus, apart from a semiconductor die or other semiconductor device component, are secured to a die or other semiconductor device component by way of a non-conductive film or die attach paste 33. Col. 3, lines 60-66; col. 4, lines 21-24, 55-56; col. 5, lines 4-6.

Independent claim 1 of the above-referenced application recites a semiconductor device for use in a stacked multi-chip assembly. The semiconductor device of claim 1 includes at least a semiconductor die and a spacer layer on at least a portion of the surface of the semiconductor die. The spacer layer protrudes from the semiconductor die "substantially a predetermined distance

that [the] semiconductor die and an adjacent semiconductor die . . . are to be spaced apart from one another . . ."

Foster lacks any express or inherent description of a spacer layer that protrudes "substantially a predetermined distance that [a] semiconductor die and an adjacent semiconductor die . . . are to be spaced apart from one another . . ." Rather, in addition to the thickness of the lead lock tape 32 that holds ILTs 20 of Foster in position relative to one another, the thickness of ILTs 20 and the thickness of one or more layers of non-conductive film or die attach paste 33 define the distance between a semiconductor die and an adjacent component, such as another semiconductor die.

Moreover, neither the lead lock tape 32 nor the ILTs 20 of Foster is "formed on at least a portion of a surface of [the] semiconductor die . . .," as required by independent claim 1. Instead, these elements are formed separately from the semiconductor die, then adhered thereto with a non-conductive film or die attach paste 33.

Further, Foster neither expressly nor inherently describes that the lead lock tape 32 includes "voids communicating with a lateral periphery thereof." While there may be voids or spacing between the ILTs 20 of Foster, the ILTs 20 are conductive structures and, thus, could not be considered to be part of a dielectric spacer layer.

It also is respectfully submitted that the assertions that the ILTs 20 of Foster are part of a dielectric spacer layer are flawed since the law that has been relied upon by the Office relates to the unpatentability of one-piece structures over similar multi-piece structures in the prior art. It does not follow from the cited case law that features of a prior art apparatus which do not correspond to claim elements (*e.g.*, ILTs 20 to the "dielectric spacer layer") may be combined with features of a prior art apparatus that do correspond to claim elements (*e.g.*, lead lock tape 32 to the "dielectric spacer layer") to provide all of the recited features of the claim elements (*e.g.*, protruding substantially "a predetermined distance that [adjacent semiconductor dice] are to be spaced apart from one another," "including voids communicating with a lateral periphery thereof"). Thus, the dielectric lead lock tape 32 of Foster cannot be combined with the conductive ILTs 20 of Foster to anticipate the dielectric spacer layer recited in independent claim 1.

For these reasons, it is respectfully submitted that Foster does not anticipate each and every element of independent claim 1 and, thus, that, under 35 U.S.C. § 102(e), independent claim 1 is allowable over Foster.

Claims 2-11, 17, and 18 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 2 is additionally allowable because Foster does not expressly or inherently describe that either the lead lock tape 32, the non-conductive film, or the die attach paste 33 thereof comprises a plurality of discrete regions.

Claim 6 is further allowable since the lead lock tape 32, non-conductive film, and die attach paste 33 of Foster do not space adjacent semiconductor dice apart from one another a predetermined distance that is about the same as or less than a distance a discrete conductive element protrudes above a surface of at least one of the adjacent semiconductor dice.

Claim 8 is also allowable since Foster neither expressly nor inherently describes that any of the lead lock tape 32, non-conductive film, or die attach paste 33 thereof comprises a pattern.

Claim 9 is additionally allowable since Foster lacks any express or inherent description that any of the lead lock tape 32, non-conductive film, or die attach paste 33 thereof comprises randomly arranged features.

Independent claim 19 recites a semiconductor device assembly that includes a first semiconductor device, a nonconfluent spacer layer that comprises dielectric material on a surface of the first semiconductor device, and a second semiconductor device positioned over the first semiconductor device and adhered to the nonconfluent spacer layer.

The assemblies of Foster that have the arrangement recited in independent claim 1 are illustrated in FIGs. 6-9C and described in the accompanying text.

Foster does not expressly or inherently describe that the lead lock tape 32 of any of these assemblies is nonconfluent (*i.e.*, does not "flow together" or does not "[m]erge[e] or [run] together so as to form a mass" (American Heritage College Dictionary, Tenth Edition)). Rather, Foster describes and depicts a lead lock tape 32 which is a confluent member which may or may not include an aperture therethrough. The non-conductive film or die attach paste 33 of Foster,

which secure the lead lock tape 32 and the ILTs 20 to semiconductor dice, are likewise depicted as comprising or forming confluent layers rather than nonconfluent layers, as required by independent claim 19.

It is, therefore, respectfully submitted that Foster does not anticipate each and every element recited in independent claim 19. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 19 is allowable over Foster.

Each of claims 20-26, 31-33, 40, and 42-44 is allowable, among other reasons, as depending either directly or indirectly from claim 19, which is allowable.

Claim 22 is also allowable because Foster does not expressly or inherently describe that either the lead lock tape 32, the non-conductive film, or the die attach paste 33 thereof comprises a plurality of discrete regions.

Claim 26 is further allowable since the lead lock tape 32, non-conductive film, and die attach paste 33 of Foster do not space adjacent semiconductor devices apart from one another a predetermined distance that is about the same as or less than a distance a discrete conductive element protrudes above a surface of at least one of the adjacent semiconductor devices.

Claim 32 is additionally allowable because Foster lacks any express or inherent description that the lead lock tape 32, non-conductive film, or die attach paste 33 thereof may comprise at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

Claim 33 is also allowable since Foster neither expressly nor inherently describes that any of the lead lock tape 32, non-conductive film, or die attach paste 33 thereof comprises a pattern.

Claim 42 is additionally allowable since Foster lacks any express or inherent description of a plurality of nonconfluent spacer layers between adjacent semiconductor devices.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1-11, 17-26, 31-33, 40, and 42-44 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Claims 12, 13, 32, and 37-39 each stand rejected under 35 U.S.C. § 103(a).

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Foster

Claims 37-39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster.

Claims 37-39 are each allowable, among other reasons, as depending either directly or indirectly from claim 19, which is allowable.

Foster, in View of Smith

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster, in view of U.S. Patent 6,049,370 to Smith, Jr. et al. (hereinafter "Smith").

Claim 12 is allowable, among other reasons, as depending from claim 1, which is allowable.

Foster, in View of Mueller

Claims 13 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Foster in view of U.S. Patent 6,316,786 to Mueller et al. (hereinafter "Mueller").

Claim 13 is allowable, among other reasons, as depending from claim 1, which is allowable.

Claim 32 is allowable, among other reasons, as depending from claim 19, which is allowable.

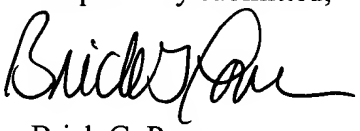
ELECTION OF SPECIES REQUIREMENT

It is respectfully submitted that independent claims 1 and 19 remain generic to all of the species of invention that were identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 14-16, 27-30, 34-36, 41, and 45-67, which have been withdrawn from consideration, should also be allowed.

CONCLUSION

It is respectfully submitted that each of claims 1-67 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing the allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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